Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-19. (Canceled)

20. (New) A microprocessor-based system, comprising:

a microprocessor;

at least one peripheral device coupled to the microprocessor via a bus;

an address map coupled to the microprocessor, the address map storing address allocated to the peripheral device to enable accesses thereto over said bus;

a peripheral control register coupled to receive peripheral control data from the microprocessor;

peripheral device disable logic coupled between the peripheral control register and to the peripheral device; and

address mapping logic coupled to the address map to automatically remove an address space allocated to a disabled peripheral device from the address map, whereby an address for the disabled peripheral device is not generated on the bus.

21. (New) The microprocessor-based system as claimed in claim 20, wherein a peripheral device may be disabled by sending a logic signal from the peripheral control register to the peripheral device disable logic associated with said peripheral device.

22. (New) The microprocessor-based system as claimed in claim 21, wherein, when said logic signal is sent from the peripheral control register to the peripheral device disable logic associated with said peripheral device, a corresponding logic signal is also sent to said address mapping logic to remove the address space for said disabled peripheral device from the address map.

23. (New) The microprocessor-based system as claimed in claim 20, having a programmable address map, wherein, when the address space for said disabled peripheral device is removed from the address map, a clock signal is automatically gated off from the peripheral device.

24. (New) The microprocessor-based system as claimed in claim 20, having a programmable address map, wherein, when the address space for said disabled peripheral device is removed from the address map, a logic signal is sent to said peripheral device disable logic to gate off the clock signal from the peripheral device, and thereby disable the peripheral device.

25. (New) The microprocessor-based system as claimed in claim 20, further comprising a clock generator configured to supply a clock signal to each peripheral device, through the associated peripheral device disable logic.

26. (New) The microprocessor-based system as claimed in claim 20, wherein the system is implemented in an integrated circuit, and wherein at least one peripheral device comprises an interface for an external device.

27. (New) A microprocessor-based system as claimed in claim 20, wherein the system is implemented in a programmable logic integrated circuit, and wherein the microprocessor is provided as an embedded circuit, while at least one of the peripheral device is implemented in programmable logic.

28. (New) An integrated circuit, comprising:

a microprocessor coupled to a peripheral device via a bus;

address mapping logic coupled to an address map for storing addresses allocated to peripheral device to enable accesses thereto over said bus; and

a peripheral control register coupled to receive peripheral control data form the microprocessor, and configured to disable a peripheral device, and

wherein, when a peripheral device is disabled, said address allocated to the disabled peripheral device is automatically removed from the address map to prevent further access attempts thereto.

29. (New) The integrated circuit as claimed in claim 28, wherein said peripheral device comprises an interface to an external device.

30. (New) The integrated circuit as claimed in claim 28, wherein said peripheral device is implemented in programmable logic.

31. (New) The integrated circuit as claimed in claim 28, wherein a peripheral device may be disabled by sending a logic signal from the peripheral control register to the peripheral device disable logic associated with said peripheral device.

32. (New) The integrated circuit as claimed in claim 31, wherein, when said logic signal is sent from the peripheral control register to the peripheral device disable logic associated with said peripheral device, a corresponding logic signal is also sent to address mapping logic to remove the address for said peripheral device from the address map.

33. (New) The integrated circuit as claimed in claim 31, further comprising a clock generator configured to supply a clock signal to the peripheral device, through the associated peripheral device disable logic.

34. (New) The integrated circuit as claimed in claim 28, wherein said address map is programmable, and wherein, when the address for a peripheral device is removed by said microprocessor from the address map, a clock signal is prevented from reaching said peripheral device to disable said peripheral devic.

35. (New) In a microprocessor-based system, comprising a microprocessor coupled via a bus to at least one peripheral device, a method of operating the system comprising:

storing in an address map at least one address corresponding to the at least one peripheral device;

disabling the at least on peripheral device; and

automatically removing from the address map an address corresponding to the disabled peripheral device, thereby preventing further access attempts thereto via the bus.

36. (New) The method as claimed in claim 35, wherein disabling the at least one peripheral device comprises supplying a first logic signal from a peripheral control register to a peripheral device disable logic associated with said peripheral device.

37. (New) The method as claimed in claim 35 wherein the disabling step further comprises automatically gating off a clock signal from the peripheral device.

38. (New) The method as claimed in claim 36, wherein the step of automatically removing comprises supplying a second logic signal corresponding to the first logic signal, to said address map to remove the address corresponding to the disabled peripheral device from the address map.